REMARKS

The Applicant thanks the Examiner for his comments in the Office Action dated October 11, 2002. A copy of the Declaration is enclosed, as requested by the Examiner. Amended drawings are enclosed, which include the Examiner's suggestion. No new matter has been added to the disclosure of the application. The drawings show every feature of the inventions specified in the claims. The proposed drawing corrections are shown in red.

The Examiner rejects claims 9 and 10 under 35 U.S.C. §103(a) as being unpatentable over Nakanishi et al. in view of Adachi et al. as applied to claims 1 and 2 above and further in view of Kinzer. The Applicant has amended claim 9 by deleting the words "to be" and adding "electrically" before connected; therefore, "connected to said pad section and to one another" is no longer intended use language and now differentiates the claimed apparatus from the prior art. Furthermore, claim 9 has been amended to incorporate the limitations of claims 1 and 2 from which claim 9 depended, putting claim 9 in independent form. Claim 10 depends from claim 9, incorporating all of the limitations of claim 9. Therefore, the Applicant respectfully submits that claims 9 and 10 are non-obvious over the prior art of record and are now in condition for allowance.

Also, it is respectfully submitted that there is no motivation to combine Nakanishi et al. and Adachi et al. Figure 12 of Nakanishi et al. does not disclose the second adhesive being electrically insulative. Indeed, Nakanishi et al. teaches that the structure of Figure 12 results in damage to the passivation layer during processing of the packaging (column 2, lines 32-36 and lines 43-50). Also, alternative processing methods are costly (column 3, lines 8-10) or lack general use properties (column 3, lines 18-22) and degrade reliability (column 3, lines 22-26). Thus, Nakanishi et al. teaches away from the structure of claim 1, and one of ordinary skill would not look to combine Fig. 12 of Nakanishi et al. with any other reference.

In addition, Kinzer teaches away from the invention as claimed in amended claim 9. Specifically, Kinzer teaches that the surface of the die ordinarily considered the top surface, which contains the heat generating junction of a power electrode faces and is connected with a conductive slug opposite of the pad of the contact frame to increase heat transfer from the heat generating junction of the power electrode (column 1, lines 48-60). Thus, Kinzer teaches away from first surfaces of first and second die each containing a power electrode electrically connected to said pad section and to one another. Therefore, there is no motivation to combine

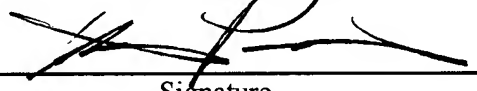
Kinzer with Nakanishi et al. Furthermore, claim 10 depends from claim 9, incorporating all of the limitations of claim 9, and claim 10 is non-obvious over the prior art for the same reasons.

The Examiner rejected claims 1, 2, 6 and 11 under 35 U.S.C. §103(a) as being unpatentable over Nakanishi et al. in view of Adachi et al. However, the lack of motivation to combine Nakanishi et al. and Adachi et al., as detailed above, applies equally well to the obviousness rejection of claims 1, 2, 6 and 11. Thus, one of ordinary skill in the art would not look to combine Figure 12 of Nakanishi et al. and Adachi et al. to obtain the invention claimed by claim 1, and claims 1, 2, 6 and 11 are non-obvious over the prior art.

The Applicant respectfully submits that all of the pending claims are now in condition for allowance. Such action is earnestly solicited.

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on December 11, 2002:

Christopher Paradies
Name of applicant, assignee or Registered Representative



Signature
December 11, 2002
Date of Signature

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Respectfully submitted,

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APPENDIX A
"Clean" Version of Each Paragraph/Section/Claim
37 C.F.R. § 1.121(b)(ii) and (c)(i)

SPECIFICATION:

Replacement for paragraph number [0023] at page 4:

[0023] In accordance with the invention, and as shown in Figures 1 and 2, the drain electrodes of two power MOSFET die 30 and 31 are conductively fixed to the opposite top and bottom surfaces of the lead frame pad 21. Thus, they can be connected by conductive adhesive layers such as layers 32 and 33 respectively in Figure 2. Layers 32 and 33 may be epoxies with silver particles loaded therein. Solder and tape can also be used. The first and second die are bonded so that they will not release from the lead frame during solder reflow. A specific embodiment connects the drains (on surfaces 34 and 35) of each of MOSFETs 30 and 31 to a common drain node D (pad 21) as shown in Figure 4. Alternatively, the two power MOSFET die 30 and 31 are MOSgated power devices and each contains a power electrode (not shown) on surfaces 34 and 35 of each of power MOSFET die 30 and 31 connect the power electrode to a common power node (pad 21).

Replacement for paragraph number [0024] at page 5:

[0024] In one specific embodiment, the source electrodes 30′, 38, 39 on the opposite surfaces 36, 37 of MOSFETs 30 and 31 and the gate electrodes 30″ on the same surfaces 36, 37 are then wire bonded to selected ones of the lead frame pins. For example, sets of wire bonds connect source electrodes 38 of die 30 to pin 23 and source electrodes 39 to pin 22 while the gate electrode of die 30 is wire-bonded to pin 26.

Replacement for paragraph number [0031] at page 6:

[0031] In Figures 5, 6 and 7, parts identical to these of Figures 1 to 4 have the same identifying numeral. The IC die 50 is connected to the bottom of pad 21 by an insulation adhesive 51 (Figure 5) such as a polyimide or the like. The IC can derive its operating power from leads 23 and 27 and has a control input terminal connected to pin 26 and an output line 52 which is internally wire bonded to the gate electrode of die 30. The source electrode 30′, 38 and 39 of die 30 may be wire bonded to one or more of the pins 22 to 29.

CLAIMS (with indication of amended or new):

9. (Twice Amended) A semiconductor device package comprising a lead frame having a conductive pad section with first and second opposite surfaces and a plurality of coplanar pin sections, a first and a second semiconductor die, each having first and second opposite surfaces at least one of said first and second opposite surfaces having a plurality of electrodes, and selected ones of said plurality of electrodes connected electrically to selected ones of said plurality of pin sections; said first surface of said first die being fixed to and connected with said first surface of said pad section; said first surface of said second die being fixed to and connected with said second surface of said pad section; an insulation housing enclosing said die and said pad section; a conductive adhesive for connecting said first surface of said first die to said first surface of said pad section; a second adhesive for connecting said first surface of said second die to said second surface of said pad section; wherein said second adhesive is electrically insulative; and wherein said pin sections extend through the surface of said insulation housing to its exterior and said first and second die are MOSgated power devices; and wherein said first surfaces of said first and second die each contains a power electrode electrically connected to said pad section and to one another.

APPENDIX B
Version with Markings to Show Changes Made
37 C.F.R. § 1.121(b)(iii) and (c)(ii)

SPECIFICATION:

Paragraph number [0023] at page 4:

[0023] In accordance with the invention, and as shown in Figures 1 and 2, the drain electrodes of two power MOSFET die 30 and 31 are conductively fixed to the opposite top and bottom surfaces of the lead frame pad 21. Thus, they can be connected by conductive adhesive layers such as layers 32 and 33 respectively in Figure 2. Layers 32 and 33 may be epoxies with silver particles loaded therein. Solder and tape can also be used. The first and second die are bonded so that they will not release from the lead frame during solder reflow. [This arrangement] A specific embodiment connects the drains [30‴, 31‴] (on surfaces 34 and 35) of each of MOSFETs 30 and 31 to a common drain node D (pad 21) as shown in Figure 4. Alternatively, the two power MOSFET die 30 and 31 are MOSgated power devices and each contains a power electrode (not shown) on surfaces 34 and 35 of each of power MOSFET die 30 and 31 connect the power electrode to a common power node (pad 21).

Paragraph number [0024] at page 5:

[0024] [The] In one specific embodiment, the source electrodes 30′, [31′] 38, 39 on the opposite surfaces 36, 37 of MOSFETs 30 and 31 and the gate electrodes 30″ [and 31″] on the same surfaces 36, 37 are then wire bonded to selected ones of the lead frame pins. [Thus] For example, sets of wire bonds connect [the] source [electrode] electrodes 38 of die 30 to [pins 22 and] pin 23 and source electrodes 39 to pin 22 while the gate electrode of die 30 is wire-bonded to pin 26.

Paragraph number [0031] at page 6:

[0031] In Figures 5, 6 and 7, parts identical to these of Figures 1 to 4 have the same identifying numeral. The IC die 50 is connected to the bottom of pad 21 by an insulation adhesive 51 (Figure 5) such as a polyimide or the like. The IC can derive its operating power from leads 23 and 27 and has a control input terminal connected to pin 26 and an output line 52 which is internally wire bonded to the gate electrode of die 30. The source electrode 30′, 38 and 39 of die 30 may be wire bonded to one or more of the pins [22 to 25] 22 to 29.

CLAIMS:

9. (Twice Amended) A semiconductor device package comprising a lead frame having a conductive pad section with first and second opposite surfaces and a plurality of coplanar pin sections, a first and a second semiconductor die, each having first and second opposite surfaces at least one of said first and second opposite surfaces having a plurality of electrodes, and selected ones of said plurality of electrodes connected electrically to selected ones of said plurality of pin sections; said first surface of said first die being fixed to and connected with said first surface of said pad section; said first surface of said second die being fixed to and connected with said second surface of said pad section; an insulation housing enclosing said die and said pad section; a conductive adhesive for connecting said first surface of said first die to said first surface of said pad section; a second adhesive for connecting said first surface of said second die to said second surface of said pad section; wherein said second adhesive is electrically insulative; and wherein said pin sections extend through the surface of said insulation housing to its exterior and [The package of claim 2,] said first and second die are MOSgated power devices; and wherein said first surfaces of said first and second die each contains a power electrode [to be] electrically connected to said pad section and to one another.